Atty. Dkt. No.: 039153-0694 (H1725)

ABSTRACT

A method of manufacturing an integrated circuit (IC) can utilize a shallow trench isolation (STI) technique. The shallow trench isolation technique can be used in strained silicon (SMOS) process.

5 Separate liners for the trench are used for NMOS and PMOS regions. The liners can induce strain in the substrate.